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PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Toshio Takayama et al

Group Art Unit: 2811

Serial No.: 10/735,886

Examiner: Nitin Parekh

Filed: December 16, 2003

P.T.O. Confirmation No.: 5693

For: SEMICONDUCTOR DEVICE HAVING A MULTILAYER INTERCONNECTION STRUCTURE AND FABRICATION PROCESS THEREOF

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Date: November 9, 2004

Sir:

This is in response to the Office Action of October 6, 2004, requiring restriction between alleged inventions under the provisions of 35 USC § 121.

In the Action, the examiner made a restriction requirement among the inventions of **Group I** drawn to a semiconductor device/system (claims 1-6 and 18); and **Group II** drawn to a method of making a semiconductor device (claims 7-17).

Applicants hereby provisionally elect **Group I , that is, claims 1-6 and 18,** for examination on the merits in this application. Applicants reserve the right to file one or more divisional applications directed to the subject matter of the non-elected claims.

Favorable consideration of the subject application is respectfully requested.

In the event this paper is not timely filed, the undersigned hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this response.

Respectfully submitted,

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